AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of fabricating a semiconductor device, the method comprising:

forming a nitride polish stop layer, at a thickness no greater than 400Å, over a semiconductor substrate;

forming an opening in the nitride polish stop layer and a trench in the substrate;

filling the trench with insulating material forming an overburden on the nitride polish stop layer; ~~and~~

polishing to form an upper planar surface stopping on the nitride polish stop layer, thereby forming a shallow trench isolation region; and

ion implanting impurities through the nitride polish stop layer to form impurity regions for source/drain regions in the semiconductor substrate adjacent the shallow trench isolation region.

2. (Original) The method according to claim 1, comprising forming the nitride polish stop layer at a thickness of 50Å to 150Å.

3. (Original) The method according to claim 1, comprising polishing to form the upper planar surface while removing no more than 20Å of the nitride polish stop layer.

4. (Original) The method according to claim 1, comprising forming a pad oxide layer on an upper surface of the semiconductor substrate, and forming the nitride polish stop layer on the pad oxide layer.

5. (Cancelled)

6. (Original) The method according to claim 5, further comprising:

removing the nitride polish stop layer;

forming a gate oxide layer on the semiconductor substrate after removing the nitride polish stop layer; and

forming a gate electrode on the gate oxide layer.

7. (Original) The method according to claim 6, further comprising etching to remove part of an upper surface of the insulating material filling the trench so that the upper surface of the insulating material is substantially coplanar with the upper surface of the semiconductor substrate before removing the nitride polish stop layer.

8. (New) A method of fabricating a semiconductor device, the method comprising:

forming a nitride polish stop layer, at a thickness no greater than 400Å, over a semiconductor substrate;

forming an opening in the nitride polish stop layer and a trench in the substrate;

filling the trench with insulating material forming an overburden on the nitride polish stop layer;

polishing to form an upper planar surface stopping on the nitride polish stop layer, thereby forming a shallow trench isolation region; subsequently

etching to remove part of an upper surface of the insulating material filling the trench so that the upper surface of the insulating material is substantially coplanar with the upper surface of the semiconductor substrate; and, subsequently,

removing the nitride polish stop layer.